

STATUS OF THE CLAIMS

The status of the claims of the current application stands as follows:

Claims 1-6: **(Canceled)**

7. **(Currently Amended)** An integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system, the integrated redundancy architecture comprising:
- a BIST for identifying and transmitting row and column addresses of ~~corresponding~~ respective-failed memory cells of embedded memory;
 - a first memory element for storing, as to-be-repaired row addresses, ones of the row addresses assigned by said BIST for repair by row redundancy;
 - a second memory element for storing, as to-be-repaired column addresses, ones of the column addresses assigned by said BIST for repair by column redundancy;
 - a third memory element for accumulating ones of the row and column addresses of the failed memory cells not already contained in said first and second memory elements and for assigning each of the ~~failed~~ row and column addresses accumulated in said third memory element a particular weight value based on the number of the failed row and column addresses already accumulated in said third memory element and the relative locations ~~of said failed row and column addresses~~ within the memory system of the row and column addresses accumulated in said third memory element; and
 - a means for:
 - determining whether the row address of a failed memory cell matches any of the to-be-repaired row addresses stored in the first memory element;
 - determining whether the column address of the failed memory cell matches any of the to-be-repaired column addresses stored in the second memory element;
 - if the row address of the failed memory cell does not match any of the to-be-repaired row addresses stored in the first memory element and the column address of the failed memory cell does not match any of the to-be-repaired column addresses stored in the second memory element, storing the row and column addresses of the failed memory cell in the third memory element;

if either the row address of the failed memory cell matches one of the to-be-repaired row ~~addresses~~ addresses stored in the first memory element or the column address of the failed memory cell matches one of the to-be-repaired column addresses stored in the second memory element, or both, then:

determining whether the row address of another failed memory cell matches any of the to-be-repaired row addresses stored in the first memory element; and

determining whether the column address of the another failed memory cell matches any of the to-be-repaired column addresses stored in the second memory element.

8. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said first, second, and third memory elements include the function of content addressable memory.
9. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said first memory element includes a register for storing row addresses that have been assigned for repair by row redundancy.
10. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said second memory element includes a register for storing column addresses that have been assigned for repair by column redundancy.
11. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said third memory element includes a register for accumulating the failed row and column addresses transmitted from said BIST.
12. **(Previously Presented)** An integrated redundancy architecture according to claim 7, further comprising a finite state machine having a decision algorithm, said finite state machine in electrical communication with said first memory element, said second memory element, and said third memory element.
13. **(Previously Presented)** An integrated redundancy architecture according to claim 12, wherein said finite state machine allocates redundancy resources of said memory system

according to said decision algorithm.

Claims 14-20: (Canceled)

21. (Currently Amended) An integrated circuit comprising:

an embedded memory system having a plurality of row and column redundancies;

a BIST for identifying row and column addresses of defective memory blocks in said embedded memory system;

a first memory element to store, as to-be-repaired row addresses, row addresses identified by said BIST to be repaired by row redundancy;

a second memory element to store, as to-be-repaired column addresses, column addresses identified by said BIST to be repaired by column redundancy;

a third memory element for accumulating ones of the row and column addresses of said defective memory block identified by said BIST that are not already stored in said first and second memory elements and assigning them a particular row or column weight value based on the number of like addresses already accumulated and still resident in said third memory element and their relative locations within the memory system; and

means for:

determining whether the row address of a failed memory cell matches any of the to-be-repaired row addresses stored in the first memory element;

determining whether the column address of the failed memory cell matches any of the to-be-repaired column addresses stored in the second memory element;

if the row address of the failed memory cell does not match any of the to-be-repaired row addresses stored in the first memory element and the column address of the failed memory cell does not match any of the to-be-repaired column addresses stored in the second memory element, storing the row and column addresses of the failed memory cell in the third memory element;

if either the row address of the failed memory cell matches one of the to-be-repaired row addressed addresses stored in the first memory element or the column address of the failed memory cell matches one of the to-be-repaired column addresses stored in the second memory element, or both, then:

determining whether the row address of another failed memory cell matches any of the to-be-repaired row addresses stored in the first memory element; and
determining whether the column address of the another failed memory cell matches any of the to-be-repaired column addresses stored in the second memory element.

22. **(Previously Presented)** An integrated circuit according to claim 21, further comprising a finite state machine having a decision algorithm, said finite state machine in electrical communication with said first memory element, said second memory element, and said third memory element.
23. **(Previously Presented)** An integrated circuit according to claim 22, wherein said finite state machine allocates redundancy resources of said memory system according to said decision algorithm.
24. **(Previously Presented)** An integrated circuit according to claim 21, wherein at least one of said first, second, and third memory elements include content addressable memory.
25. **(Previously Presented)** An integrated circuit according to claim 21, wherein said first memory element includes a register for storing said failed row addresses.
26. **(Previously Presented)** An integrated circuit according to claim 21, wherein said second memory element includes a register for storing said failed column addresses.